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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/886,972	06/25/2001	Yoshihisa Kato	740819-566	7056

22204 7590 05/28/2003

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EXAMINER
PHAM, LY D

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,972	KATO ET AL.	
	Examiner	Art Unit	
	Ly D Pham	2818	

-- The MAILING DATE of this communication appears on th cov r sh t with th corr spond nce addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 2* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Transitional After Final Practice

1. Applicant's second request for reconsideration, filed May 08, 2003, entered in Office paper no. 9, with respect to the rejection(s) of claim(s) 1 and 2 under the remarks have been fully considered and are persuasive. Therefore, the final rejection has been withdrawn and prosecution is reopened for the present application. However, upon further consideration, a new ground(s) of rejection is made in view of the newly found references provided below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al. (US Pat 5,196,912) in view of Nakamura et al. (Japanese Pat Sho 61-61297).

Regarding **claims 1 and 2**, Matsumoto et al. disclose a method for driving a semiconductor memory composed of a field effect transistor having a gate electrode formed on a ferroelectric film, comprising the steps of:

writing a data in said semiconductor memory by changing a polarized state of said ferroelectric film by applying a voltage to said gate electrode (abstract: ..., data can be written, erased, and read out by selectively applying an electric field to the gate insulating film).

Although Matsumoto et al. did disclose the step of reading a data according to the claim; however, Nakamura et al. have shown the step of reading a data written in the semiconductor memory by detecting a current change appearing between a drain and a source of the field effect transistor ... (page 6, lines 4 – 18), wherein magnitude of the voltage applied between the drain and the source of said field effect transistor in the step of reading a data is set within a range where a drain-source current of said field effect transistor increases as a drain-source voltage thereof increases (linear/non-saturation operating region of the FET, page 6, lines 18 – 20. See also claims 1 and 2, pages 2 – 3).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine reading method shown by Nakamura et al. to the data writing method of Matumoto et al. for small current detection and high speed readout (Nakamura, page 3).

4. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (US Pat 6,285,577 B1) in view of Homma et al. (US Pat 5,163,022).

Regarding **claims 1 and 2**, Nakamura disclose a method for driving a semiconductor memory composed of a field effect transistor having a gate electrode formed on a ferroelectric film, comprising the steps of:

writing a data in said semiconductor memory by changing a polarized state of said ferroelectric film by applying a voltage to said gate electrode (abstract: invert polarization of the ferroelectric layer for data write and read opearations).

Although Nakamura did not disclose the step of reading a data in the semiconductor memory as claimed; however, Homma et al. have shown the step of reading a data written in the semiconductor memory by detecting a current change appearing between a drain and a source of said field effect transistor ..., (col. 6, line 66 – col. 7, line 2), wherein magnitude of the voltage applied between the drain and the source of said field effect transistor in the step of reading a data is set within a range where a drain-source current of said field effect transistor increases as a drain-source voltage thereof increases (abstract: sense amplifier detects the difference between the currents flowing in selected BIT lines to read out stored information .... See also col. 6, lines 41 - 44).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to incorporation the memory readout method shown by Homma et al. to the disclosure of Nakamura, to provide high speed, low power, and high integration density (Homma et al.: abstract).

5. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al. (US Pat 6,498,362 B1) in view of Hidaka (US Pat 6,172,918 B1).

Regarding **claims 1 and 2**, Forbes et al. disclose a method for driving a semiconductor memory composed of a field effect transistor having a gate electrode formed on a ferroelectric film, comprising the steps of:

writing a data in said semiconductor memory by changing a polarized state of said ferroelectric film by applying a voltage to said gate electrode (col. 8, lines 42 – 55).

Although Forbes et al. did not disclose the step of reading a data in the semiconductor memory as claimed; however, Hidaka has shown the step of reading a data written in the semiconductor memory by detecting a current change appearing between a drain and a source of said field effect transistor ..., wherein magnitude of the voltage applied between the drain and the source of said field effect transistor in the step of reading a data is set within a range where a drain-source current of said field effect transistor increases as a drain-source voltage thereof increases (col. 13, lines 18 - 30).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the reading method shown by Hidaka to the invention of Forbes et al. so that the read gate amplifiers can be optimized (Hidaka: col. 13, lines 30 – 37).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

12. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

13. Any inquiry concerning this communication on earlier communications from the examiner should be directed to Ly Pham, whose telephone number is 703-305-4862. The examiner can normally be reached on Monday – Friday from 8:30am to 5:00pm, alternate Friday off. The examiner's supervisor, David Nelms, can be reached at 703-308-4910. The fax number for the organization where this application or proceeding is assigned is 703-308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Ly Pham

May 19, 2003

David Nelms
Supervisory Patent Examiner
Technology Center 2800